EE 4610 Communication Electronics 2012 Spring Semester

1. Course Description:

This introductory course will cover system-level and circuit design issues relevant to wireline communication systems.

2. Text books:

Handouts and technical papers

3. Teaching Method:

Lecture: 3 hours

Outside study: 4 hours

3. Evaluation:

Homework: 40% (no late homework)

Midterm: 30%

Case study and presentation: 30%

4. Prerequisites:

Microelectronics

Analog Integrated Circuits Analysis and Design

Digital Circuit Analysis and Design

5. Tentative Syllabus:

2/28	3/1:	Introduction	
3/6	3/8:	Channel characteristics	
3/13	3/15:	Transmitter circuits I	
3/20	3/22:	Receiver circuits I	
3/27	3/29:	Tx equalization	(FIR/FFE)
4/3	4/5:	Rx equalization I	(FIR/CTLE)

4/10	4/12:	Rx equalization II (DFE)
4/17	4/19:	Midterm
4/24	4/26:	Clocking circuits I (PLL)
5/1	5/3:	Clocking circuits II (DLL)
5/8	5/10:	Clocking circuits III (phase interpolator)
5/15	5/17:	Source synchronous clocking
5/22	5/24:	Clock-and-data recovery
5/29	5/31:	Clock distribution I
6/5	6/7:	Clock distribution II
6/12	6/14:	Presentations