National Tsing Hua University
Department of Electrical Engineering
EE4292 IC Design Laboratory (積體電路設計實驗), Spring 2014

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Attention

1) This laboratory course is an implementation-oriented one and includes intense homework assignments, midterm exam, and term project. It is only suitable for the students who already have basic knowledge about electronics, logic design, and IC design.
2) From this semester, this course will focus only on **digital cell-based IC** design flow, instead of the mixed digital and analog flow in the previous years.

Prerequisites: Electronics, Logic Design, Introduction to Integrated Circuits Design

Course Description

Learning cell-based IC design flow is like learning how to drive an airplane. You may not need to know every detail of aerodynamics and mechanics, but you had better understand what each number on the control panel means and why the red right is on! Operating the CAD tools is also like driving an airplane. It is never easy to land the plane safely, and make the chip really work.
This course teaches not only how to use the million-dollar CAD tools but also the concept and technology behind them. You will learn and operate a basic but complete cell-based design flow with an advanced cell library, which includes Verilog RTL, synthesis, P&R, and verification.

Teaching Method

Lectures (1-3 hours) are given every week at DELTA 209R and followed by hands-on labs (1-3 hours) at DELTA 219R with remote EE workstation. The connection between the tools is very strong, so intense practice of each taught tool is highly required. There will be four homework assignments and a term project. Labs will teach you how to use the tools in a basic way, and you need to keep practicing on the HWs and term project on your own. The basics of hardware description language and RTL-to-netlist synthesis are especially essential, so there will be a midterm exam on them.
The advanced Synopsys SAED 28nm cell library will be used throughout this course, which includes standard cell, I/O pad, and SRAM compiler.
(***Note***: The library and tools are all very precious resources. Without CIC and the generous software providers, we will be unable to access them. So, please use them very carefully and only for this course.)

Evaluation

Lab (10%)
Homework (40%)
Midterm (20%)
Term Project (30%)

Note:

1. For each lab, there will be checkpoints for TA to check.
2. One original work deserves only one credit. For example, if five students deliver the same (or very similar) results for homework or midterm, the grades will be averaged by five. If the original work deserves 100 points, each one will get only 20 points. Rebuttal is allowed.
3. Two home assignments for Verilog coding, one for synthesis, and one for P&R. The grading equation for late delivery is

   $$\text{New grade} = (\text{original grade}) \times 0.9^{(\text{delievery date} - \text{due date})}$$

4. Midterm: Open book, 1-hour paper-based test + 2-hour workstation-based test
5. Project: Build your own chip or advanced design flow. Details will be disclosed later. No late delivery is allowed.

Syllabus

Date	Week	Lecture Topic	Lab	HW out	HW due
2/19	1	Overview: Syllabus and Introduction	Workstation and text editor		
2/26	2	Verilog (I): Verilog Fundamentals (CVLM module 2~8)	Verilog simulator (NC-Verilog)		
3/5	3	Verilog (II): Verilog for Verification (CVLM module 9~11, 19~21)	Testbench debugging and writing	1	
3/12	4	Verilog (III): Verilog for Synthesis (CVLM module 12~17)	Debugging tools (Verdi)		
3/19	5	Verilog (IV): RTL Coding Guidelines	nLint, RTL simulation and debugging	2	1
3/26	6	Verilog (V): SRAM and Selected Topics	Memory compiler and integration		
4/2	7	Synthesis (I): Synopsys Design Compiler	Design Compiler (DesignWare)		2
4/9	8	Synthesis (II): Synopsys Design Compiler	Design Compiler (SRAM)	3	
4/16	9	Synthesis (III): Optimizing RTL for Synthesis **Project Annoucement**	Coding for synthesis and optimization		
4/23	10	**Midterm Exam**			3
4/30	11	Logic Equivalence Check: Cadence Conformal LEC	LEC		
5/7	12	Place & Route (I): Automatic Physical Implementation	IC Compiler - Floorplan		
5/14	13	Place & Route (II): Placement *Project Progress Report*	Placement w/ SRAM	4	
5/21	14	Place & Route (III): Clock-tree Synthesis and Routing	CTS and routing		
5/28	15	Layout Verification and Post-layout Operations	IC Compiler verification tools		4
6/4	16	Cell-based Design Flow Revisit	Post-layout simulation and LEC		
6/11	17	**Project Presentation (Report Due)**			

CVLM: Cadence Verilog Lecture Manual

Five weeks on Verilog, three on Synthesis, three on P&R, and two on Verification.

Tool

HDL simulation: NC-Verilog
Synthesis: Design Compiler
P&R: IC Compiler
Debug/Verification: Verdi, nLint, LEC

Textbook

None.

References

Lecture notes will be provided every week, which are based on:

- Cadence Lecture Manuals for Verilog and LEC (only in paper format)
- M. Keating and P. Bricaud, *Reuse Methodology Manual for System-on-a-Chip Designs*, Springer, 2007.
- CIC course lecture notes and labs
- Personal experience and other resources

Note

The SAED library and Cadence lecture notes are only accessible and available for the students who are enrolled in this course. Any misuse of them is prohibited, including copy and redistribution.

Course Link

iLMS website: http://lms.nthu.edu.tw/course/17272

Teaching Assistant

劉詒軒、李易庭、柯佑蓉、邱柏捷