National Tsing Hua University
Department of Electrical Engineering
EE4292 IC Design Laboratory (積體電路設計實驗), Fall 2015

Instructor:	**Chao-Tsung Huang (黃朝宗)**
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Course Description

This course provides a basic but complete digital cell-based design flow with an advanced cell library. It is about how to implement your ideas into silicon through many abstraction layers (Idea → Hardware Description Language → Gate-level Netlist → Physical Layout) and also how to make sure the function and performance are met. Verilog HDL, logic synthesis, and physical placement and routing will be taught for the implementation of abstraction transitions, and essential verification methods will be also introduced.

Learning cell-based IC design flow is like learning how to drive an airplane. You may not need to know everything in detail but had better understand what each number on the control panel means and why the red right is on! It is never easy to land the plane safely or make the chip really work. This course will not only teach how to use the million-dollar CAD tools but also introduce the concept and technology behind them.

Prerequisites: Logic Design, Introduction to Integrated Circuits Design, Electronics

Teaching Method

Lectures (1-3 hours) are given every week at DELTA 201R and followed by hands-on labs (1-3 hours) at workstation classroom (EECS 406). The connection between the tools is very strong, so intense practice of each taught tool is highly recommended. There will be four homework assignments and one term project. Labs will teach you how to use the tools in a basic way, and you need to keep practicing on the HWs and term project on your own. The basics of Verilog HDL and logic synthesis are especially essential, so there will be a midterm exam on them.

The Synopsys SAED 28nm cell library will be used throughout this course.

(***Note***: The library and tools are all very precious resources. Without CIC and the generous software providers, we will be unable to access them. So, please use them very carefully and only for this course.)

Evaluation

Lab (5%)
Homework (45%)
Midterm (20%)
Term Project (30%)

Note:

1. For each lab, there will be checkpoints for TA to check.
2. One original work deserves only one credit. For example, if five students deliver the same (or very similar) results for homework or midterm, the grades will be averaged by five. If the original work deserves 100 points, each one will get only 20 points. Rebuttal is allowed.
3. Four home assignments will be given. The grading equation for late delivery is
   $$\text{New grade} = (\text{original grade}) \times 0.9^{(\text{delievery date} - \text{due date})}$$
4. Midterm: Open book, 0.5~1-hour paper test + 1.5~2-hour on-line test (2.5 hours in total).
5. Project: Build your own chip for some digital functions. Details will be disclosed on 11/4. **No late delivery is allowed**.

Syllabus

Date	Week	Lecture Topic	Lab	HW out	HW due
9/16	1	Overview: Syllabus and Introduction	Workstation and text editor		
9/23	2	Verilog (I): Verilog Fundamentals (CVLM module 2~8)	Verilog simulator (NC-Verilog)		
9/30	3	Verilog (II): Verilog for Verification (module 9~11, 19~21)	CPU Intro, Testbench debugging and writing	1	
10/7	4	Verilog (III): Verilog for Synthesis (module 12~16)	Debugging tools (Verdi)		
10/14	5	Verilog (IV): System and RTL Coding Guidelines	nLint, RTL simulation and debugging	2	1
10/21	6	Design Example: Discrete Consine Transform	Line-based image processing		
10/28	7	Synthesis (I): Synopsys Design Compiler	Design Compiler	3	2
11/4	8	Synthesis (II): Synopsys Design Compiler	DesignWare, Coding for synthesis	4	3
11/11	9	Optimization for Synthesis and Selected Topics **Project Annoucement**	Coding for optimization		
11/18	10	*No Class (NTHU Sports Day)*	*No lab*		
11/25	11	**Midterm Exam** *Project Team Up*			4
12/2	12	Logic Equivalence Check: Cadence Conformal LEC	LEC	5	
12/9	13	Place & Route (I): Physical Design Flow	IC Compiler - Floorplan		5
12/16	14	Place & Route (II): Synopsys IC Compiler *Project Progress Report*	Power plan, placement, CTS and routing		
12/23	15	Place & Route (III): Layout Verification Cell-based Design Flow Revisit	DRC/LVS, netlist simulation, LEC, power analysis		
12/30	16	*No Class*	*Project Consulting*		
1/6	17	**Project Presentation (Report Due)**			

CVLM: Cadence Verilog Lecture Manual

Tool

HDL simulation: NC-Verilog
Synthesis: Design Compiler
P&R: IC Compiler
Debug/Verification: Verdi, nLint, LEC

Textbook

None.

References

Lecture notes will be provided every week, which are based on:

- Cadence Lecture Manuals for Verilog and LEC (only in paper format)
- M. Keating and P. Bricaud, *Reuse Methodology Manual for System-on-a-Chip Designs*, Springer, 2007.
- CIC course lecture notes and labs
- Personal experience and other resources

Note

The SAED library and Cadence lecture notes are only accessible and available for the students who are enrolled in this course. Any misuse of them is prohibited, including copy and redistribution.

Course Link

http://lms.nthu.edu.tw/course/23058

Teaching Assistant

陳立得、程韋翰、黃立仁、蕭裕霖、楊博翔、楊舒雯