PME320900 邏輯設計與應用

Logic Design & Applications

Teaching Goals: 本課程旨在介紹數位邏輯電路的基本特性及設計，並提供設計數位系統所使用的基本原理與概念

Learning Goals: 學生可培養基本數位邏輯電路設計的能力，並具備進階課程或實作的基礎

Course Outline: 課程內容包括：

數位系統的基本特性
數字及資料表示系統和轉換
布林代數與邏輯閘
布林代數表示式之化簡
卡諾圖之應用
多層邏輯閘電路
組合邏輯電路設計
多工器，解碼器，以及可程式化邏輯元件（PLD）
序向邏輯電路：閂鎖器和正反器
暫存器和計數器

When: 2nd semester, 2016, T 10:10-12:00, Th 10:10-11:00 (3 credits)

Where: 工程一館 201

Handouts: can be downloaded by the student at iLMS e-learning platform (http://lms.nthu.edu.tw/).

Assignments and Grading: Quiz: 10 quizzes, 40% (5 % each) (The lowest two scores will be discarded)

Midterm Exam: 30%

Final Exam: 30%

Instructor: 陳致真 副教授 / Chihchen Chen, Associate Professor (x62403, rm. 311, Delta Hall, chihchen@mx.nthu.edu.tw)

Office Hours: by appointment

Teaching Assistant: TBD

Prerequisites: NA

Textbook: C. H. Roth, Jr. and L. L. Kinney, *Fundamentals of Logic Design*, 7th edition, Cengage Learning, 2013.

References:

1. M. M. Mano and M.D. Ciletti, *Digital Design*, 4th edition, Prentice-Hall, 2007.
2. T. L. Floyd, *Digital Fundamental*, 10th Edition, Prentice Hall, 2008.
3. S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd Edition, McGraw-Hill, 2014.

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wks	**Tuesdays**	**Thursdays**	**theme**	**Reading**
1	02/16/2016	02/18/2016	**Introduction** *Number Systems and Conversion*	Unit 1
2	02/23/2016	02/25/2016	**Boolean Algebra**	Unit 2 & 3
3	03/01/2016	03/03/2016	**Boolean Algebra**	Unit 2 & 3
4	03/08/2016	03/10/2016	**Application of Boolean Algebra**	Unit 4
5	03/15/2016	03/17/2016	**Karnaugh Maps**	Unit 5
6	03/22/2016	03/24/2016	**Karnaugh Maps**	Unit 5
7	03/29/2016	03/31/2016	**Multi-level Gate Circuits**	Unit 7
8	04/05/2016	04/07/2016	**Multi-level Gate Circuits**	Unit 7
9	04/12/2016	04/14/2016	**Combinational Circuit Design**	Unit 8
10	04/19/2016	04/21/2016	**Combinational Circuit Design**	Unit 8
11	04/26/2016	04/28/2016	**Multiplexers, Decoders, and Programmable Logic Devices (PLDs)**	Unit 9
12	05/03/2016	05/05/2016	**Midterm exam** *covers Unit 1~8 (except Unit 6)*	
13	05/10/2016	05/12/2016	**Multiplexers, Decoders, and Programmable Logic Devices (PLDs)**	Unit 9
14	05/17/2016	05/19/2016	**Latches and Flip-Flops**	Unit 11
15	05/24/2016	05/26/2016	**Latches and Flip-Flops**	Unit 11
16	05/31/2016	06/02/2016	**Registers and Counters**	Unit 12
17	06/02/2016	06/09/2016	**Registers and Counters**	Unit 12
18	06/13/2016		**Final exam** *covers Unit 9, 11 & 12*	