



# Semiconductor Memories

# ENE 637000

## Semiconductor Memories 半導體記憶體

### CLASS INFORMATION

- Professor: 林崇榮
- TA: TBD
- Class time/room: 台達館 R212
- Textbook: Handouts
- FTP: [well.ee.nthu.edu.tw](http://well.ee.nthu.edu.tw) ; Login: ene63700 PWD: TBD

# Course Description

In this course, lessons consisting of VLSI semiconductor memory cells and technology by lectures and assigned projects, which developing students' professional VLSI knowledge acquired in the previous VLSI device class. Students learn to know the DRAM, SRAM and Flash technologies. They also learn to design more cell operations, processes and layout details. Extended VLSI integration technology is also addressed and introduced. Cell design and integration will be taught in class and assigned in homework. Memory cell and array for development and production will be drafted for students and aspects of the VLSI industry will be discussed.

# Course Outcomes

- ❑ Understand VLSI Integration Technology
- ❑ Understand DRAM/SRAM/FLASH Technology, Cell Layout, and Integration Process
- ❑ Create Basic Cell and Operation from VLSI Process according to Principles of Charge Storage
- ❑ Execute the TCAD or Spice Simulation Project for the Optimization of a Cell Design
- ❑ Measure and Operate Cell Performance and Characteristics Properly
- ❑ Develop Memory Architecture from Read and Write the Bit Cell Developed in High Density Memories
- ❑ Apply Basic Cell Technology and Layout to Form More Complex Cell to Cell Interactions
- ❑ Manipulate Different Memory Bitline and Wordline and Peripheral Circuit to Compose a New Memory Chip

# Semiconductor Memories

- **SRAM:** operation principle, cell structures, TFT loads and fabrication, etc.
- **DRAM:** operation principle, cell structures and technologies, sense amplifier design, architecture and interface, etc.
- **Flash:** operation principles, cell structures, process technologies, and reliability concerns for ROM, PROM, EPROM, EEPROM, Flash, etc.

# Class Syllabus and Schedule

	<b>Subject</b>	<b>Syllabus</b>	<b>Week</b>
<b>Part 1</b>	<b>Introduction</b>	<b>Memory Concept</b>	<b>1</b>
<b>Part 2</b>	<b>DRAM</b>	<b>DRAM Concept and Operation</b>	<b>2</b>
		<b>Trench DRAM Technologies</b>	<b>3</b>
		<b>Stack DRAM Technologies</b>	<b>4</b>
		<b>EXAM</b>	<b>5</b>
<b>Part 3</b>	<b>SRAM</b>	<b>SRAM Concept and Operation</b>	<b>6</b>
		<b>4T/TFT/6T/8T SRAM Technologies</b>	<b>7</b>
		<b>EXAM</b>	<b>8</b>
<b>Part 4</b>	<b>Flash Memory</b>	<b>ROM / EEPROM</b>	<b>9</b>
		<b>NOR Flash Memory</b>	<b>10</b>
		<b>NAND Flash Memory</b>	<b>11</b>
		<b>EXAM</b>	<b>12</b>
<b>Part 5</b>	<b>New Memories</b>	<b>RRAM and MRAM</b>	<b>13</b>
		<b>PCRAM and FeRAM</b>	<b>14</b>
		<b>EXAM</b>	<b>15</b>

# Grading Policy

- 40% - Homework and Report
- 60% - Exams