EE5285 Wireline Communication Integrated Circuits **2021 Fall Semester**

這個課不給加簽。
因應防疫，9/21 前的課程 (第一週) 將以預錄的方式，放置於 Youtube 平台，同學們需於 9/15 之前，將你的 gmail address 寄給助教 (林毅承 yichenglin249@gmail.com)，我們會開放權限，並於上傳後公布於課程網頁，讓同學們自行觀看。
另外由於疫情發展的不確定性，本課程學期成績以 5 次作業計算，沒有期中/期末考試。

1. Course Description:

This introductory course will cover system-level and circuit design topics relevant to wireline communications, including basic communication standards, channel characteristics, modulation/demodulation schemes, synchronization, channel equalizations, and key functional modules and the corresponding design considerations.

2. Textbooks:

- Handouts and technical papers

3. Key references:

- S.H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*, John Wiley & Sons, 2009.
- B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw Hill, 2003.
- W. Dally and J. Poulton, *Digital Systems Engineering*, Cambridge University Press, 1998.
- H. Johnson & M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993.

4. Teaching Methods:

- Lecture: 3 hours
- Outside study: 4 hours

5. Evaluation:

- Homework: 100% 5 assignments (20% each)

6. Class Webpage: NTHU eeclass system 數位學習平台 (https://eeclass.nthu.edu.tw)

7. Instructor:

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8. Teaching Assistants:

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9. Tentative Schedule:

Week#	Month	Day (Tuesday)	Day (Wednesday)	Topics
1	September	14	15	Introduction
2		21 中秋節	22	Channel characteristics
3		28 教師節	29	
4	October	5	6 HW#1 due	Transmitter circuits
5		12	13	
6		19	20	Receiver circuits
7		26	27 HW#2 due	
8	November	2	3	Receiver equalization
9		9	10	
10		16	17 全校運動會	Transmitter equalization
			HW#3 due	
11		23	24	
12	December	30	1	Phase-locked loops
13		7	8 HW#4 due	Clock-and-data recovery
14		14	15	
15		21	22	
16		28	29 HW#5 due	

- Please contact TAs for EE workstation account application