課程簡述 (Brief course description)

The goal of this course is to help students understand how to accelerate design of the complex electronics and intelligent systems. Besides, through this course, students can get the essential components of the challenges of latest system level design from all aspects of Chips/Chiplet/IP, advanced package design, to thermal aware electrical design. This course will focus on System-In-Package and “More than Moore” 3D-IC related design and sign-off methodology.

教學方式 (Teaching Method)

Lectures.

教學進度(Syllabus)

This course will include 6 major topics dividing into 2 semesters and provide student essential capabilities to understand the challenges and requirement in each design phases for advanced design methodologies. They are:

1. Overall System Level Design Planning and EDA (Electronic Design Automation)
2. Digital Design and Sign-off
3. Custom, Analog and RF Design
4. RF and Simulation with DRC/LVS
5. SiP, System-in-package (Modifying Components and Netlist/Setting Design Rules), Design Verification and Manufacturing Output
6. Routing and High-Density Interconnect with Simulation

Week/ Date	Topics	Hours		Teaching Method	Instructor
		Lecture	Exam		
1 9/15	Custom IC, Analog and RF Design -- Advanced Nodes and Layout Verification	3		Lecture and case studies	Analog, RF and Mixed Signal design
2 10/6	IC Package Design and Analysis -- SiP, System-in-package (Modifying Components and Netlist/Setting Design Rules)	3		Lecture and case studies	System level and Package design
3 10/27	IC Package Design and Analysis -- Design Verification and Manufacturing Output	3		Lecture and case studies	System level and Package design
11/17	Midterm Examination		1	Multi-selection problems	
4 11/17	Routing and High-Density Interconnect with Simulation – SI/PI	2		Lecture and case studies	Simulation for system level design
5 12/8	SI/PI Analysis -- Model generation and analysis using SPICE, 3D-EM	3		Lecture and case studies	Simulation for system level design
6 12/29	System level analysis and sign-off -- 3D solver, Thermal solver and rule-based checking	2		Lecture and case studies	Simulation for system level design
12/29	Final Examination		1	Multi-	

				selection problems	
	TOTAL	16	2		

成績考核(Evaluation)

* Attendance 10%
* In-class activity 10%
* Exam1 40%
* Exam2 40%