課程簡述 (Brief course description)

This course will focus on “More than Moore” 3D-IC and System-In-Package design, simulation, and sign-off methodology. The goal of this course is to help students understand how to implement a complex electronics system based on intelligent SDA (System Design Automation) technology. Besides, through this course, students can get the essential components of the challenges of latest system level design from all aspects of advanced packaging design and thermal aware electrical analysis.

教學方式 (Teaching Method)

Lectures

教學大綱 (Syllabus)

This course will include 6 major topics dividing into 2 semesters and provide student essential capabilities to understand the challenges and requirement in each design phases for advanced 3D-IC package design methodologies. They are:

1. Introduction to advanced packaging technology and System Design Automation (SDA) design environment
2. System-in-package (SiP) design flow and layout verification
3. Power delivery network (PDN) modeling and power integrity (PI) analysis
4. Full flow (IC-Package-PCB) signal integrity (SI) analysis in frequency and time domain with IBIS model
5. System level electrothermal (E/T) co-simulation and sign-off
6. Wafer-level probe card and IC test load board design and verification

Week/ Date	Topics	Hours		Teaching Method	Instructor
		Lecture	Exam		
1 3/8	Advanced packaging technology and System Design Automation (SDA) design environment – Advanced packaging chronicle and SDA solution	3		Lecture and case studies	Wilbert Chen
2 3/22	System-in-package (SiP) implementation and verification – Design flow	3		Lecture and case studies	AE (TBD)
3 4/12	Power delivery network (PDN) modeling and power integrity (PI) analysis – PI simulation flow from IC to PCB.	2		Lecture and case studies	AE (TBD)
4/12	Midterm Examination		1	Multiple choice question	
4 5/3	Full flow (IC-Package-PCB) signal integrity (SI) analysis in frequency and time domain with IBIS model	3		Lecture and case studies	AE (TBD)

	– SI simulation flow from IC to PCB.				
5 5/17	[Cadence Taiwan office visit]* System level electrothermal (E/T) co-simulation and sign-off – Thermal solver and rule-based checking	3		Lecture and case studies	Wei-Te Cheng, PE
6 5/31	Wafer-level probe card and IC test load board design and verification – full flow design methodology	2		Lecture and case studies	Wilbert Chen
5/31	Final Examination		1	Multiple choice question	
	TOTAL	16	2		

成績考核(Evaluation)

- Attendance 30%
- In-class activity 10%
- Exam1 30%
- Exam2 30%

*[Cadence Taiwan office visit – schedule plan] - note would be removed after delivery
Location: Cadence Taiwan Zhubei office, 3F
9:00-9:10 Check-in
9:10-9:15 Welcome Remark
9:15-9:30 Cadence Opening Talk
9:30-12:00 Lecture Course
12:00-13:00 Lunch Time